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PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10022438	FILING DATE 12/20/2001	CLASS 714	SUBCLASS 726	GAU 2133	EXAMINER TABONE
**APPLICANTS: Matsushita Yusuke;					
**CONTINUING DATA VERIFIED:					
** FOREIGN APPLICATIONS VERIFIED: JAPAN 2000-387597 12/20/2000					
PG-PUB DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>			
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no		35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no		ATTORNEY DOCKET NO NEC01P202	
Verified and Acknowledged Examiners's initials					
TITLE: Master-slave-type scanning flip-flop circuit for high-speed operation with reduced load capacity of clock controller					
U.S. DEPT. OF COMM./PAT. & TM.-PTO-436L (Rev. 12-94)					

NOTICE OF ALLOWANCE MAILED		Assistant Examiner		CLAIMS ALLOWED	
				Total Claims	Print Claim for O.G.
ISSUE FEE		Primary Examiner		DRAWING	
Amount Due	Date Paid			Sheets Drwg.	Figs. Drwg.
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE		Application Examiner	
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